REMARKS

Reconsideration and allowance of the subject application in view of the following remarks is respectfully requested.

Claims 1, 2 and 4-20 remain pending in the application.

Applicant's undersigned attorney wishes to thank Examiner Le for the courtesies extended during the personal interview conducted on January 4, 2007.

Applicant filed a Request for Continued Examination on December 6, 2006 together with a request to consider amendment previously filed on November 6, 2006. This amendment is Supplemental to the Amendment filed on November 6, 2006 and provides a written explanation of questions asked during the personal interview.

The major difference between the present invention and the prior art is the limitation in claim 1 "wherein a length of the evolution of N_a is variable and dependent on the value of N_b"". The Examiner suggested that we explain how this operates and is supported in the specification.

As the Examiner conceded in the Office Action dated July 7, 2006, Petersson et al. does not disclose that the synthesizer is a fractional step-locked loop synthesizer for providing fractional frequency steps.

The Examiner attempts to overcome this deficiency using the fractional step synthesizer technique disclosed in Fig. 2 of the present application and admitted to be prior art. However, this is not the same as the invention recited in claim 1 of the present application.

The fractional frequency step synthesizer illustrated in Figure 2 is a block diagram of a 160-320 MHz synthesizer. The technique consists in obtaining a dynamic variation in the N division rank so as to generate, for example, a mean value N comprising a fractional part. For example, if one out of ten times, the division is performed by N+1 instead of by N, the mean value N is equal to (N+1)/10. Since the rate of variation of N is far greater than the band of the feedback control loop, the VCO is offset by 1/10 of the frequency Fref. This results in a phase variation $2\pi/N$ at the phase/frequency comparator. This technique gives rise to parasitic lines at the output of the VCO. For a triple fractional step, which reduces the level of these parasitic lines, this variation goes to $6\pi/N$.

This variation must be kept below 120° especially if the phase comparator used is a diode-based mixer type of phase comparator associated with a frequency-searching device. This is to the use of minimum division ranks equal to about 10.

The synthesizer has a VCO covering the 160-320 MHz frequency band. The VCO divided by N is compared with a reference frequency of 20 MHz. A control signal N/N+1/N+2 brings about variations, at a rate of 20 MHz, in the N division rank so as to generate steps at 100th of the value of the reference frequency (a double fractional step is used with modulo 2 equal to 4 and 25 so as to benefit from an additional attenuation on the first three fractional lines).

However, this method has major drawbacks:

1) The VCO must cover a one-octave band, and this means that it is difficult to make,

2) The N divider too covers one octave, inducing a variation by 2 in the feedback loop gain, and this variation gets combined with the possible variations of slopes of the VCO and leads to increased complexity, because these variations have to be compensated for in order to maintain the switching time and the level of the parasitic lines throughout the frequency range,

3) The switching time of the synthesizer is limited because the control loop band must be below the value of the first fractional line (200 KHz in the example given) to be able to benefit from an additional attenuation of this line through the transfer function of the phase loop,

4) Since the minimum division rank is close to 10 and since the divider must cover one octave, the result is an increase of at least 26 dB in the phase noise as compared with the technological noise of the dividers.

The technique of the fractional synthesis was introduced for the first time into US Patent No. 3,928,813 of A. Kingsford-Smith on December 23, 1975 and entitled "Device for Synthesizing Frequencies which are rational multiples of a fundamental Frequency". Since this date, numerous publications and patents were allowed on this subject.

In fact Peterson was well aware of the technical problem to be resolved in the present patent application (see page 2 line 16-31 of the present patent application)

1) The difficulty realizing the VCO is mentioned in column 2, line 1-4 of Peterson;
2) The necessity of fast switching time is described in column 2, line 22-25,
3) The need of a low phase noise and low spurious us described in column 2, line 22-25.

In 1992, date of the Publication of the Patent of Petersson, the problem previously mentioned was known. Since this time, no document has disclosed or suggested the characteristics recited in amended claim 1.

Applicant submits that the present invention is new and inventive in view of the prior art.

Moreover, the method according to the present patent application and recited in claim 10 allows a faster switching time (because greater loop bandwidth described in the present patent application) and also lower phase noise and lower spurious lines (because division ranks of the loop divider in the present patent application are lower than those of Petersson).

Applicant submits the following explanation of what is called "evolution of Na" in the present patent application. In the present invention there is a triple variation attached to the divider of loop Na. The counting device recited in claim 1 is described on page 6, line 33, page 7 line 2 of the present specification. Figure 6 of the present application shows clearly that the value Na may vary from 15 to 21: it is the first variation of Na that can be qualified as static and corresponding to the phase lock-in progress of phase loop (as in Petersson).

There is then a second variation of Na, that one is dynamic, because it is processed at the rate of the frequency of comparison of loop phase, that is 144 Mhz. It means that every 6.94 ns, the value of Na is modified by 0,1 or 2 units thanks to the thread of a signal control named N/N+1/N+2. This dynamic variation corresponds to the fractional functioning of the synthesizer. The fraction step Na of the loop divider thus varies form 0 to 2 units at the rate of frequency 144 Mhz (reference frequency of the comparator of phase). This variation is cyclic (it takes place according to a periodic sequence) that is why in the present patent application it is the question of the cycle of evolution of Na.

By contrast, according to the devices of the prior art, the length of this cycle is constant. In the present application, the length of this cycle varies by what constitutes the 3rd variation concerned to the divisor Na. The length of this cycle is chosen by a table according to the value of the divisor Nb (see for example in Figure 6) In this example each of the lengths of cycle expressed in number of period of Fref=144 MHz is the product of prime number among them. The divider Nb may be adjusted and can take the values 9, 10, 12 or 15 for the example of the Figure 6. Applicant submits that the technical teaching of Petersson does not disclose or suggest the limitations recited in claim 1.

In summary, the inventiveness of the present patent application is notably:

1) varying the length of the cycle of the command N / N+1 / N+2 /... of the divider Na and making this length variable according to the rank Nb of the output divider.

2) to give a method of choice of the values of Nb and the ratio Fref/Δ F so that the different lengths of cycle correspond to multiple integers of the reference frequency Fref of the phase comparator of the loop.

In the device according to the invention, the length of the cycle of evolution of Na is variable and dependent on the value Nb (division value of the variable-rank divider on page 6 lines 14-16). In Figure 6 and the description thereof the modulo corresponds to the length of the cycle and is dependent of Nb.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

Early issuance of a Notice of Allowance is courteously solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE HAUPTMAN & BERNER, LLP

Kenneth M. Berner

Kenneth M. Berner
Registration No. 37,093

USPTO Customer No. 33308
1700 Diagonal Road, Suite 300
Alexandria, VA 22314
(703) 684-1111
(703) 518-5499 Facsimile
Date: February 22, 2007
KMB/iyr